ABSTRACT

To demodulate the RDS signal, the stereo-multiplex signal is multiplied in a first branch by the in-phase component of an oscillator, filtered by a low-pass filter while decimated in its sampling rate and filtered by a high-pass filter, while in a second branch it is multiplied by the quadrature component of the oscillator, filtered by a low-pass filter, decimated in its sampling rate, and filtered by a high-pass filter. An error signal to control the oscillator is calculated from the high-pass-filtered signals and the RDS bit clock. A clock generator generating the RDS bit clock is controlled by the first high-pass-filtered signal and by the oscillator. An RDS decoder, to whose input the first high-pass-filtered signal is applied, and an arithmetic unit which calculates the error signal from the high-pass-filtered signals and from the RDS bit clock are both clocked by the clock generator. The RDS data are retrievable from the output of the RDS decoder.